

Semester Thesis / Master Thesis

Start date : as soon as possible

Topic: *Image Processing on FPGA: Contour Detection*

Goals

- Develop a prototype with FPGA board and Conventional Camera;
- Characterize the implementation of Counter Detection algorithm on FPGA and GPU;
- Produce a Scientific Paper

Requirements:

- Basic knowledge in Computer Vision, Electronics (FPGA), and HDL (Verilog or System Verilog)

Expected results:

- Semester Thesis / Master Thesis
- Following our internal evaluation, the candidate may be funded, on a merit basis, to present the results of the work at a world-class international conference

Supervisor:



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